# 4.5.12 – 184 PIN DIMM FAMILY SUPPLEMENTARY DESIGN STANDARDS

**BACKGROUND INFORMATION:** The 184 Pin DIMM Module family consists of numerous configurations using SDR and DDR SDRAM devices. These consist of Unbuffered, and Registered designs. Complete Standards for Unbuffered SDR and Unregistered DDR devices have been published in chapter 4.5 of this Standard. Additional Buffered and Registered DIMMs can be achieved using the same pinouts with the addition of a few supplementary signals to control the buffering and registering functions.

This section contains standards defining various aspects of additional 184P DIMM configurations.

The contents of this Section are as follows:

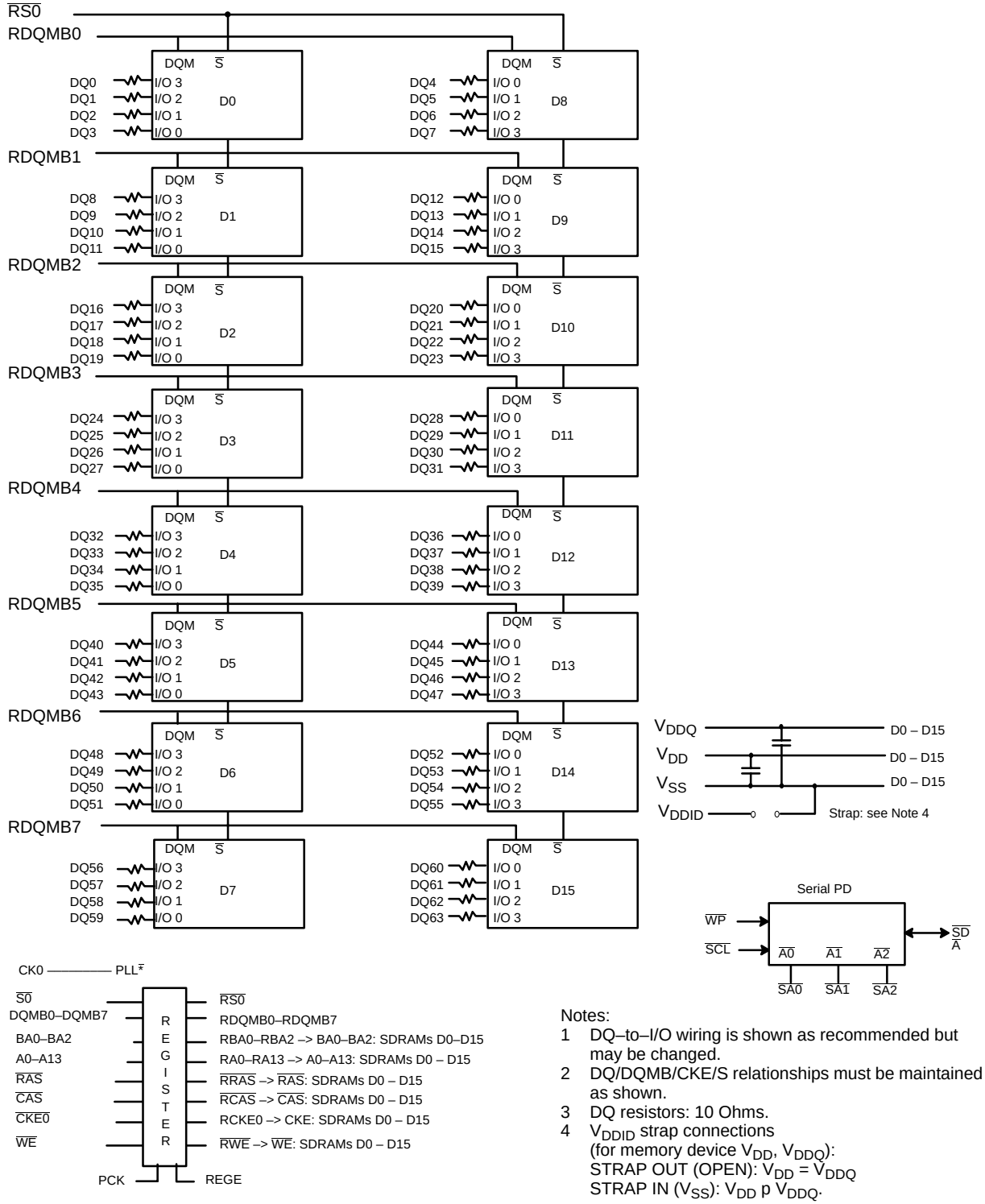
Section 1 gives a series of 18 **Block Diagrams** for an SDR Registered DIMM sub–family.

Section 2 contains **Clock Topology** layouts for DDR Registered DIMM and DDR Unbuffered DIMM.

Section 3 contains a **PINOUT** for the DDR Registered DIMM member of the family.

## 4.5.12.1 – 184 PIN SDR Registered DIMM Block Diagrams

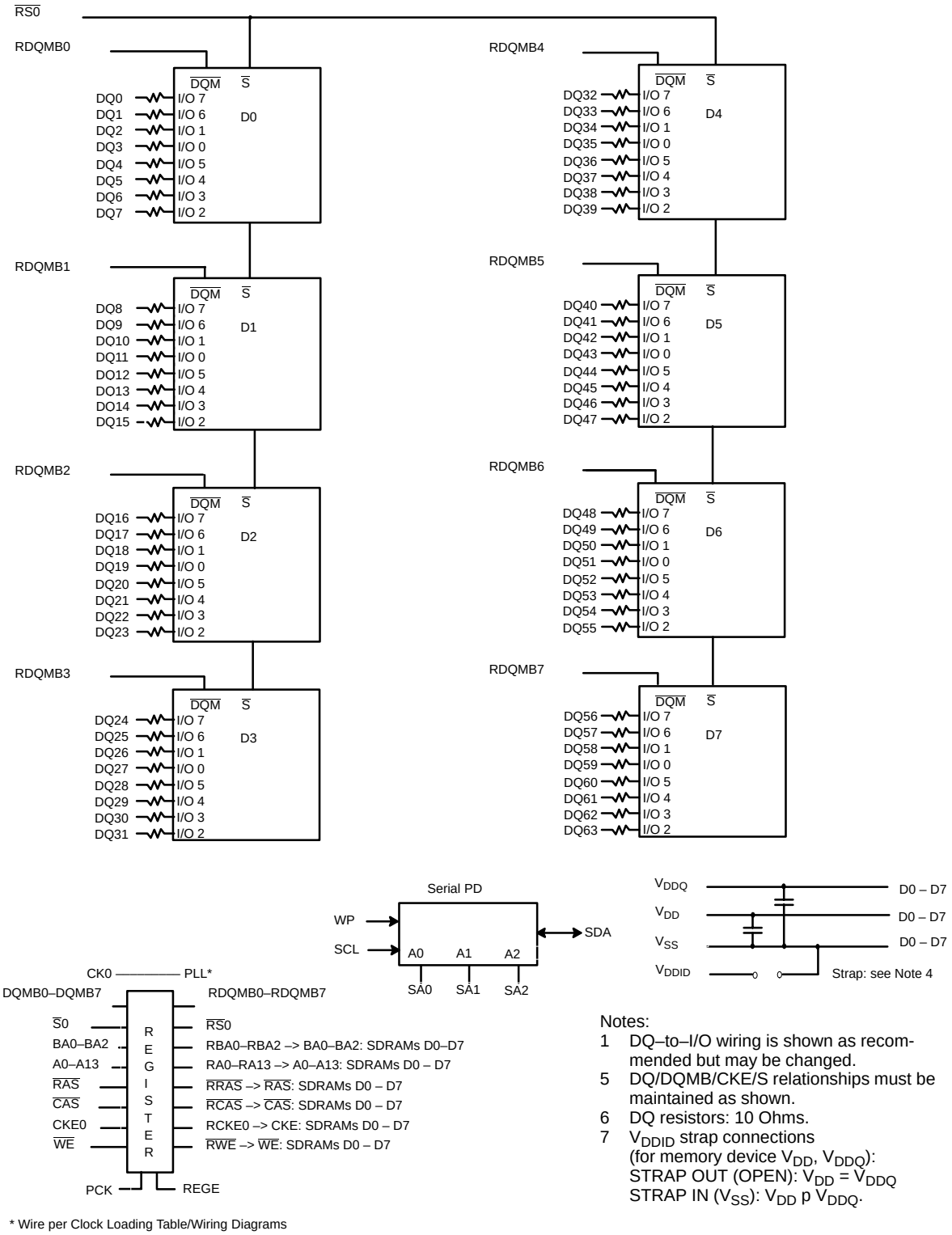
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.12–A through 4.5.12–P




Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections
(for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD}$ þ $V_{DDQ}$.

* Wire per Clock Loading Table/Wiring Diagrams

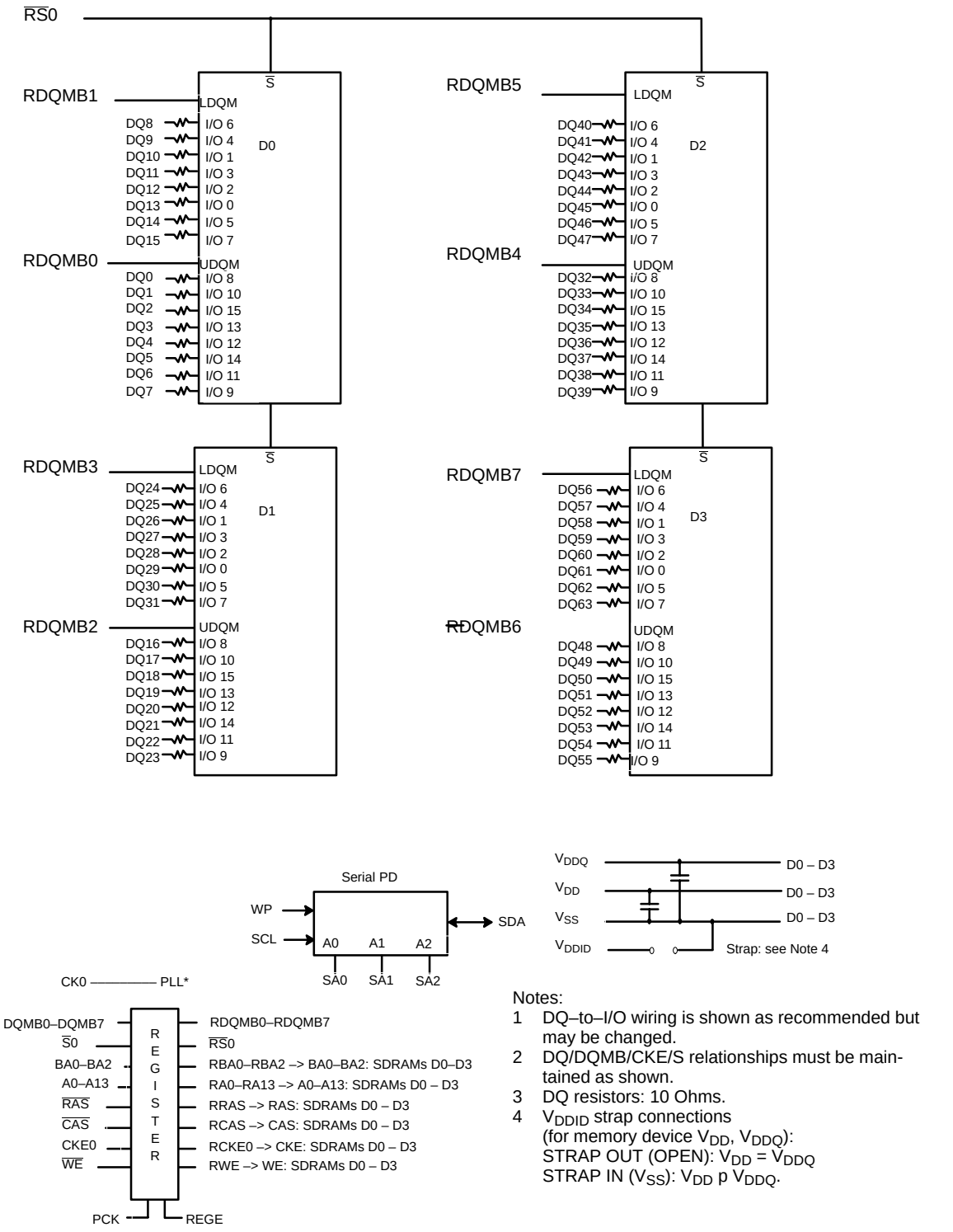
**FIGURE 4.5.12–A**
**184 PIN X64 SDR REGISTERED SDRAM DIMM (1 BANK, X4 SDR SDRAMS)**




Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
5 DQ/DQMB/CKE/S relationships must be maintained as shown.
6 DQ resistors: 10 Ohms.
7 $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

* Wire per Clock Loading Table/Wiring Diagrams

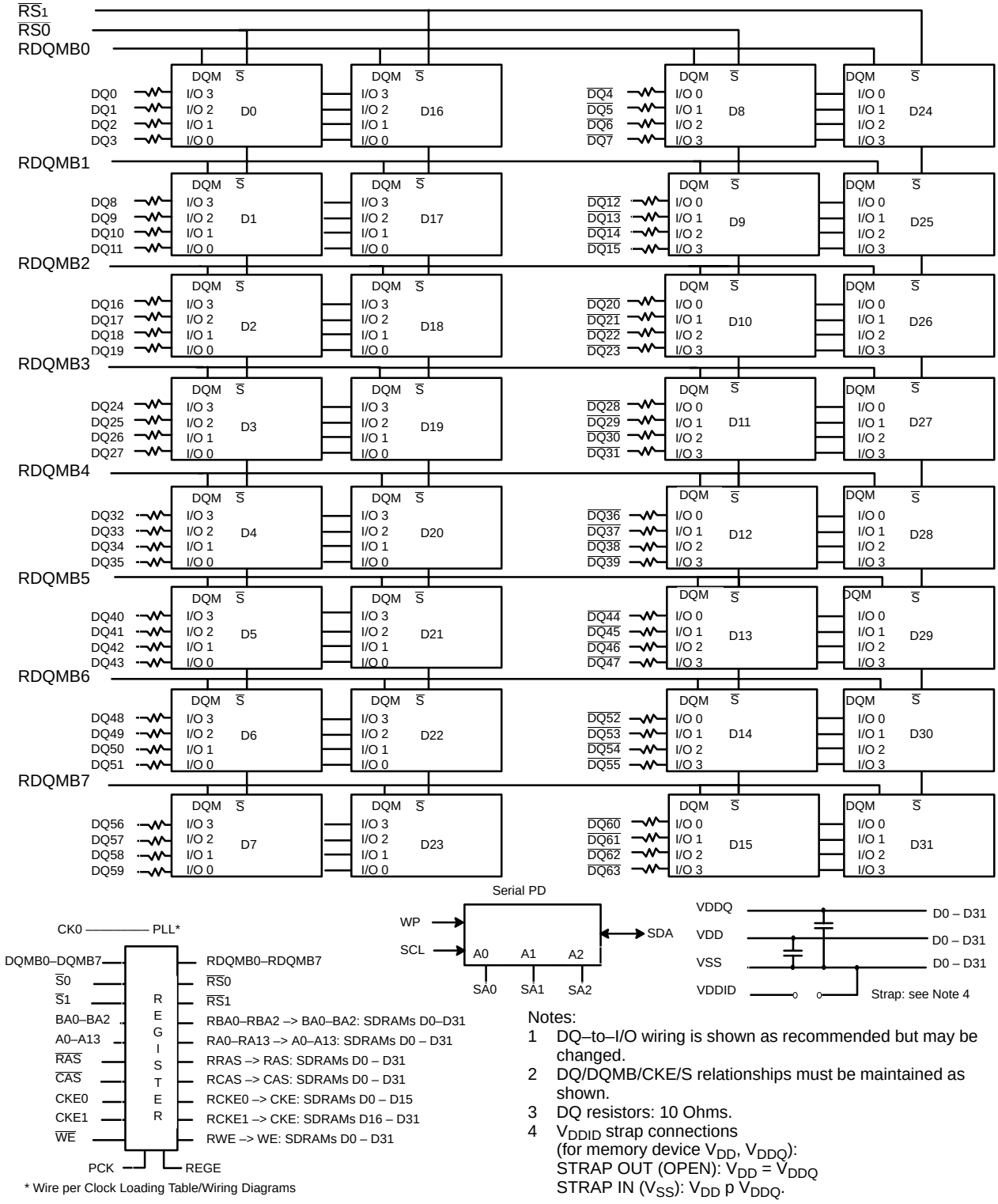
## FIGURE 4.5.12–B
## 184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (1 BANK, X8 SDR SDRAMS)




Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

* Wire per Clock Loading Table/Wiring Diagrams

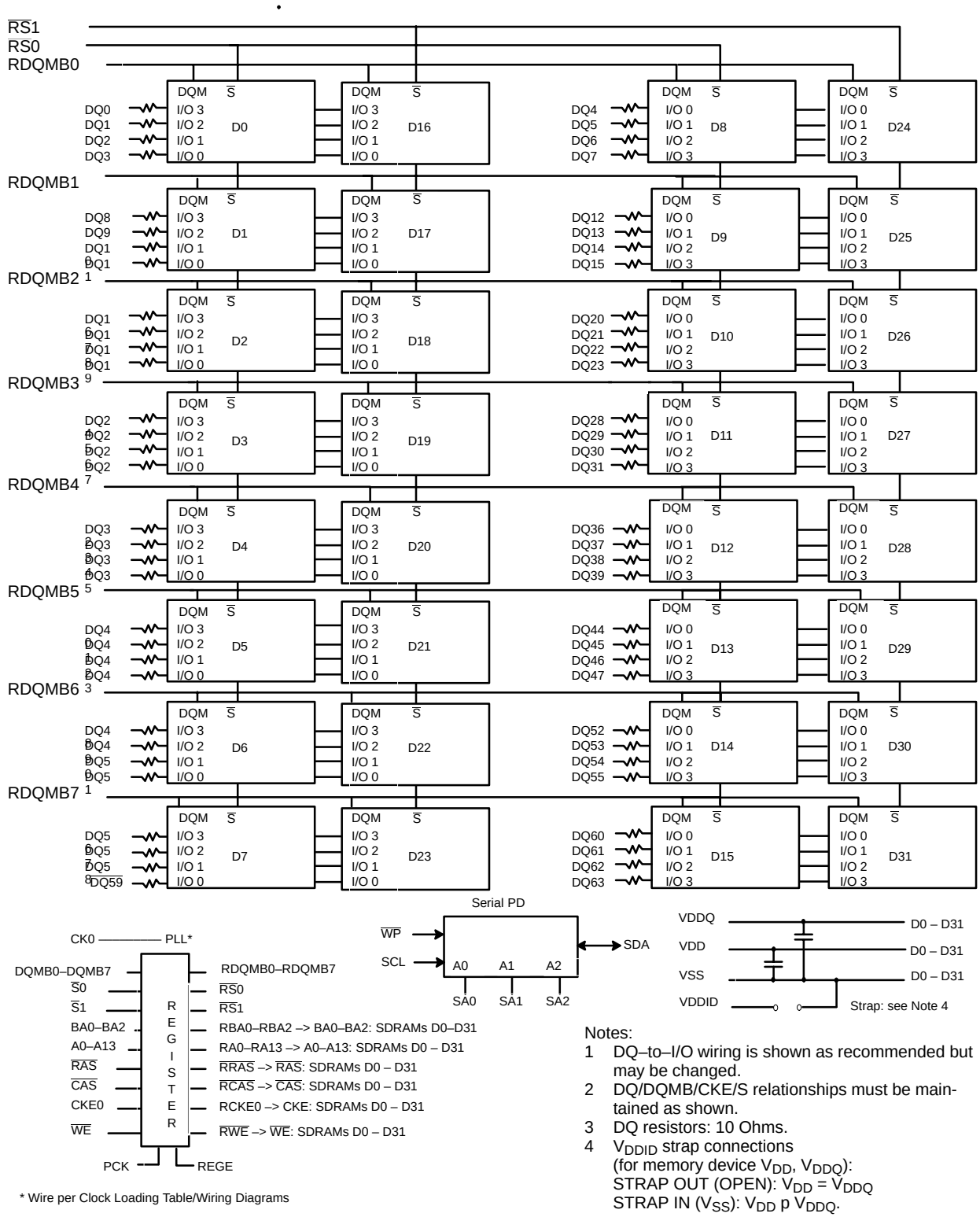
## FIGURE 4.5.12–C
## 184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (1 BANK, X16 SDR SDRAMS)




* Wire per Clock Loading Table/Wiring Diagrams

Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections
(for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

**FIGURE 4.5.12–D**
**184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM**
**(2 BANKS, X4 SDR SDRAMS WITH DOUBLE CKE)**




* Wire per Clock Loading Table/Wiring Diagrams

Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

**FIGURE 4.5.12–E**
**184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM**
**(2 BANKS, X4 SDR SDRAMS WITH SINGLE CKE)**

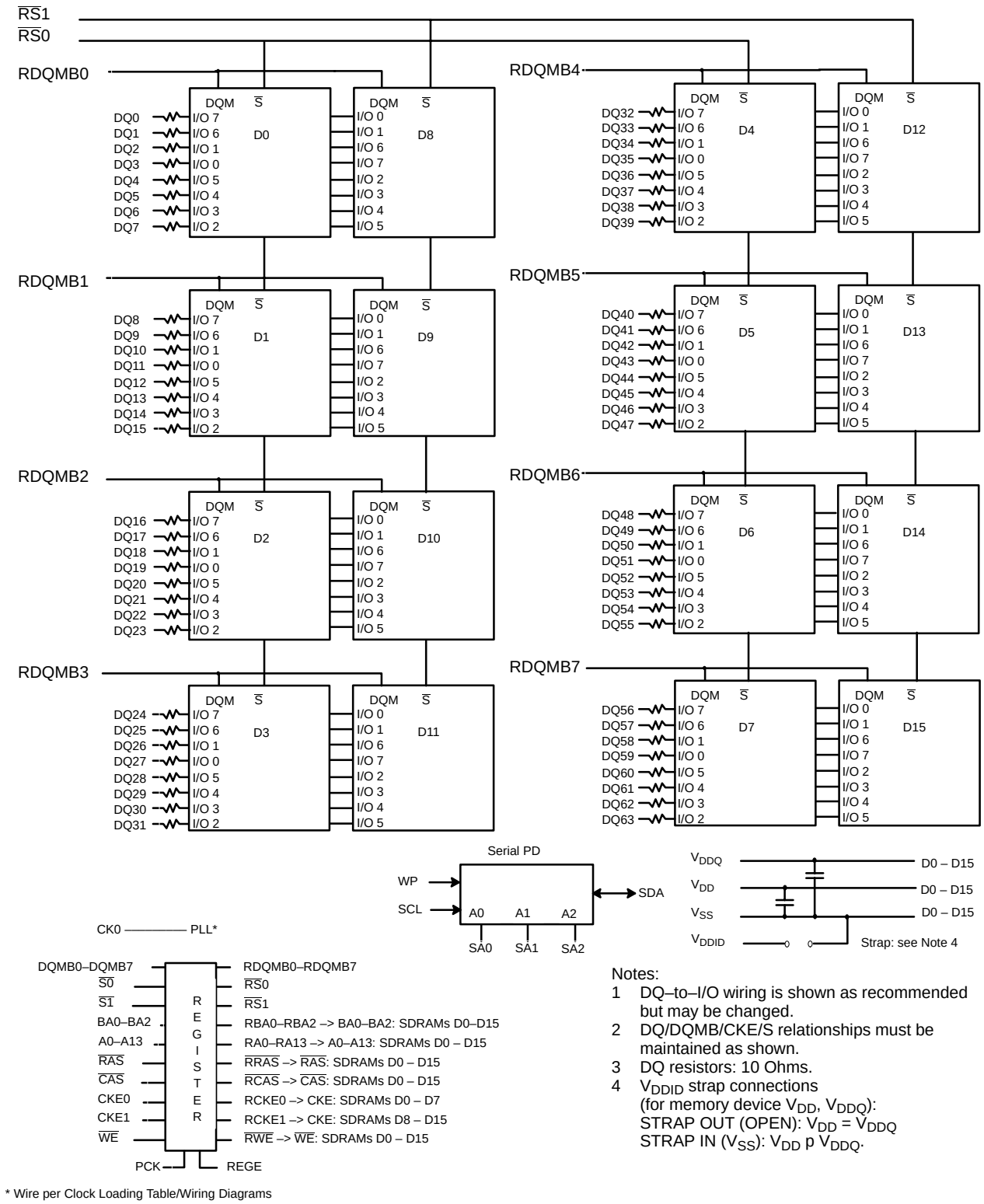
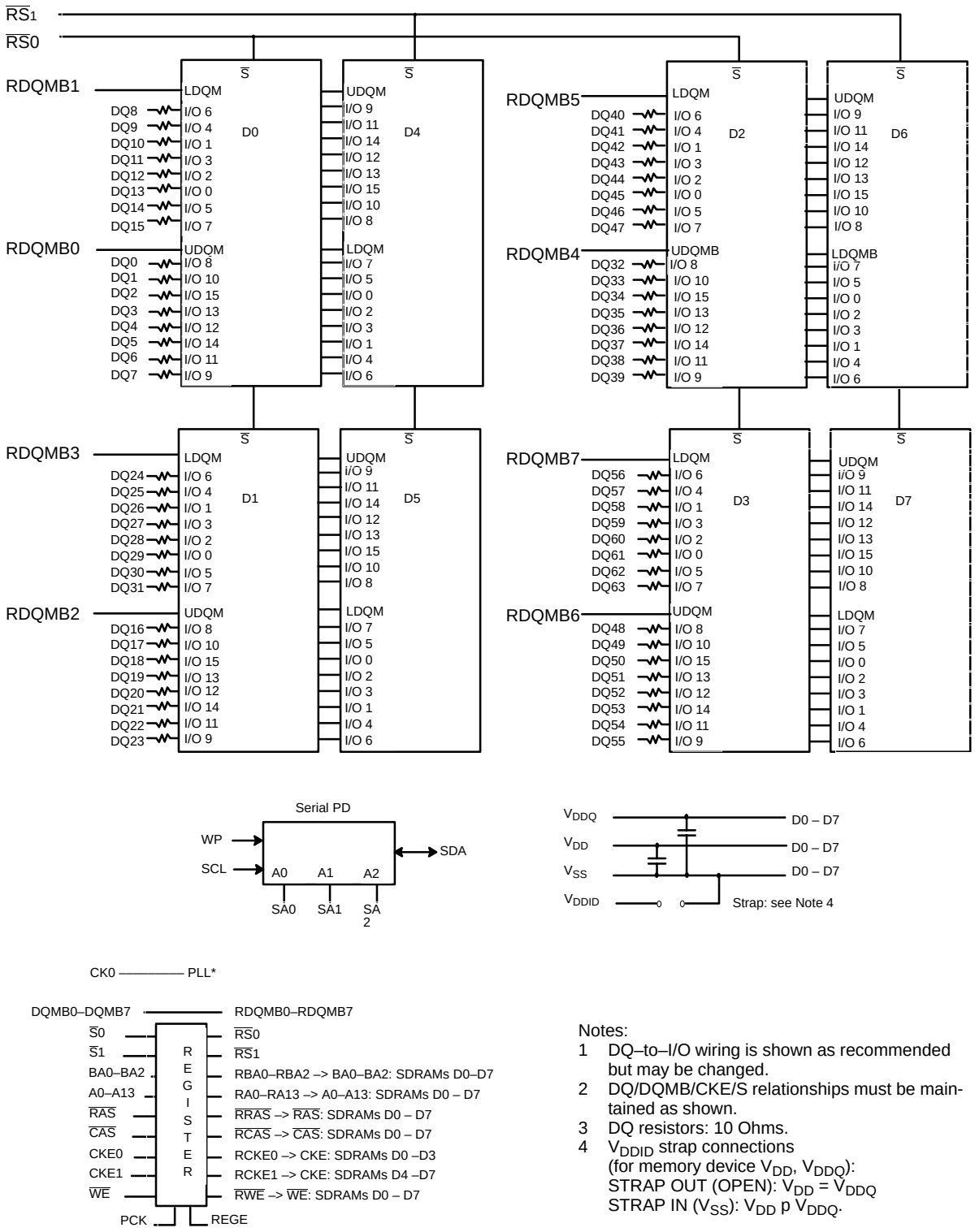


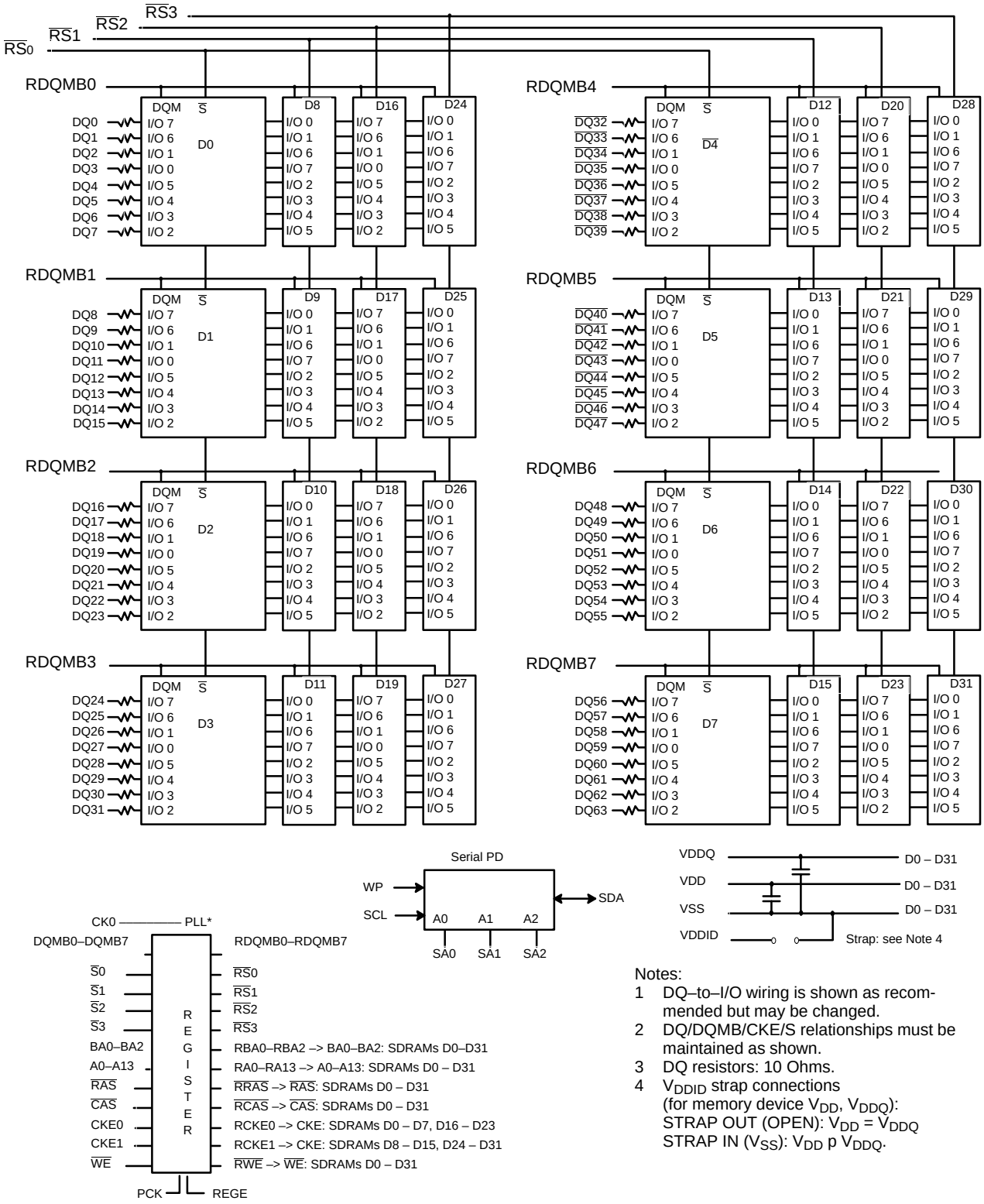

**FIGURE 4.5.12–F**
**184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (2 BANK, X8 SDR SDRAMS)**




Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

* Wire per Clock Loading Table/Wiring Diagrams

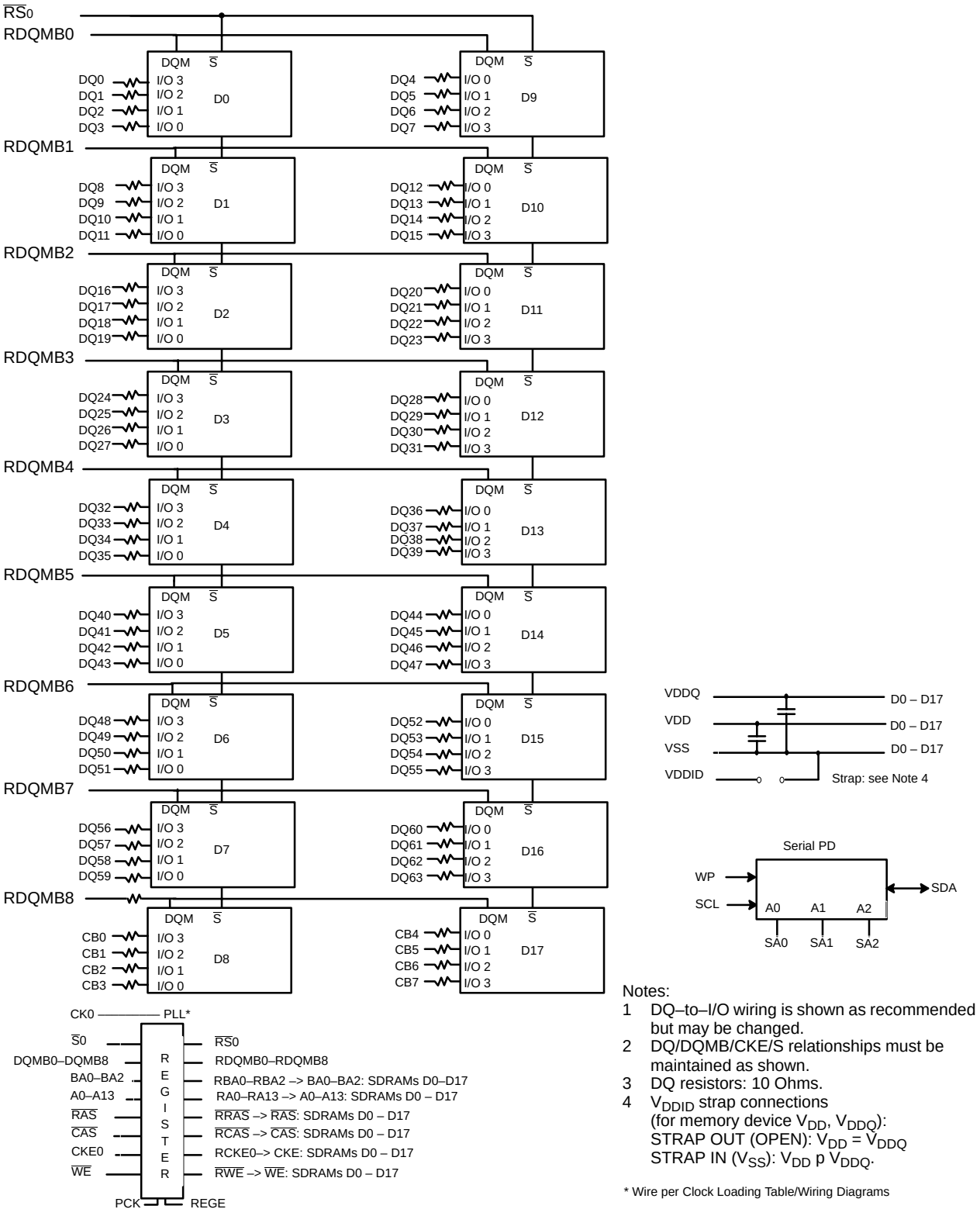
# FIGURE 4.5.12–G
# 184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (2 BANK, X16 SDR SDRAMS)




Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN ($V_{SS}$): $V_{DD}$ þ $V_{DDQ}$.

* Wire per Clock Loading Table/Wiring Diagrams

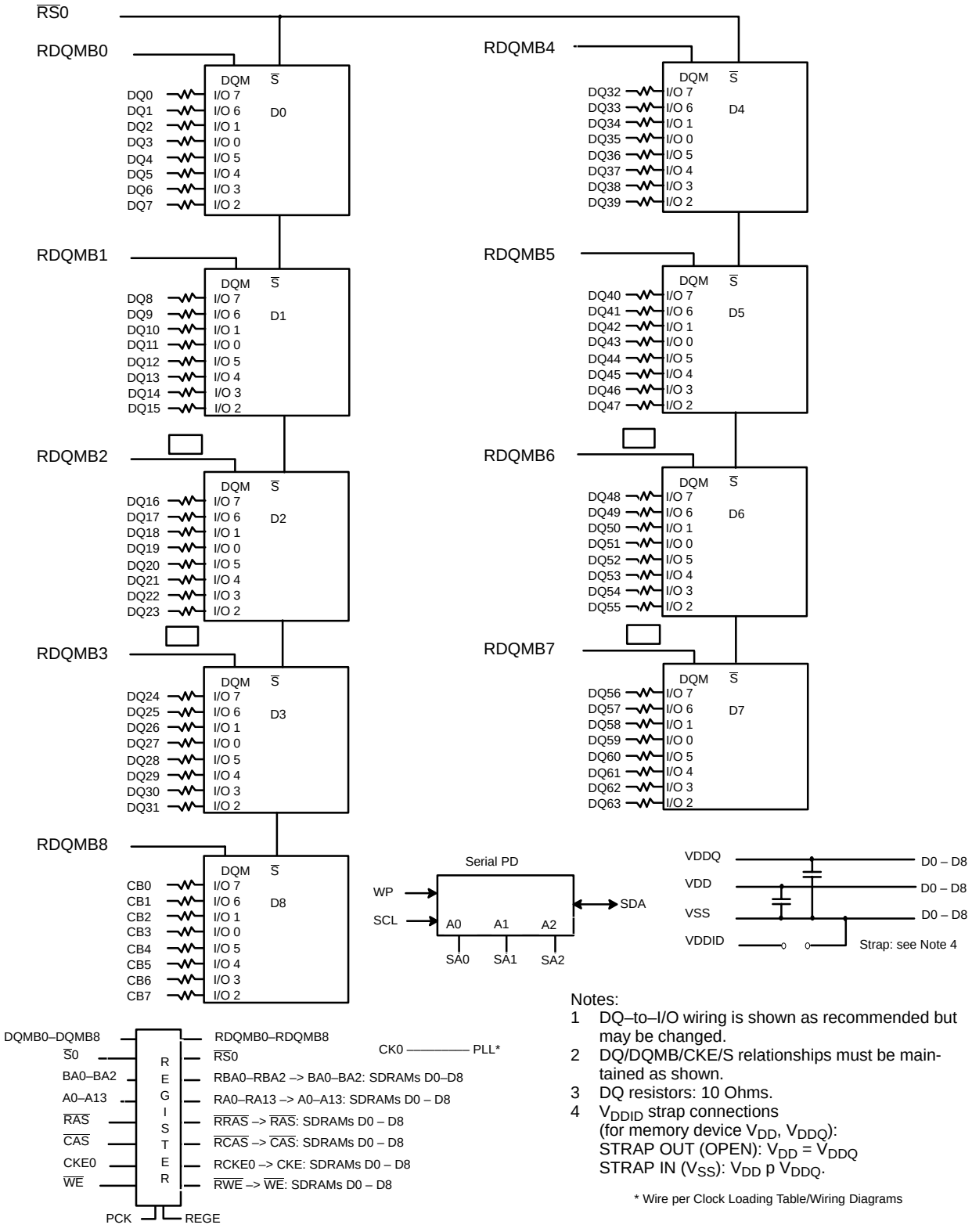
**FIGURE 4.5.12–H**
**184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (4 BANK, X8 SDR SDRAMS)**




Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

* Wire per Clock Loading Table/Wiring Diagrams

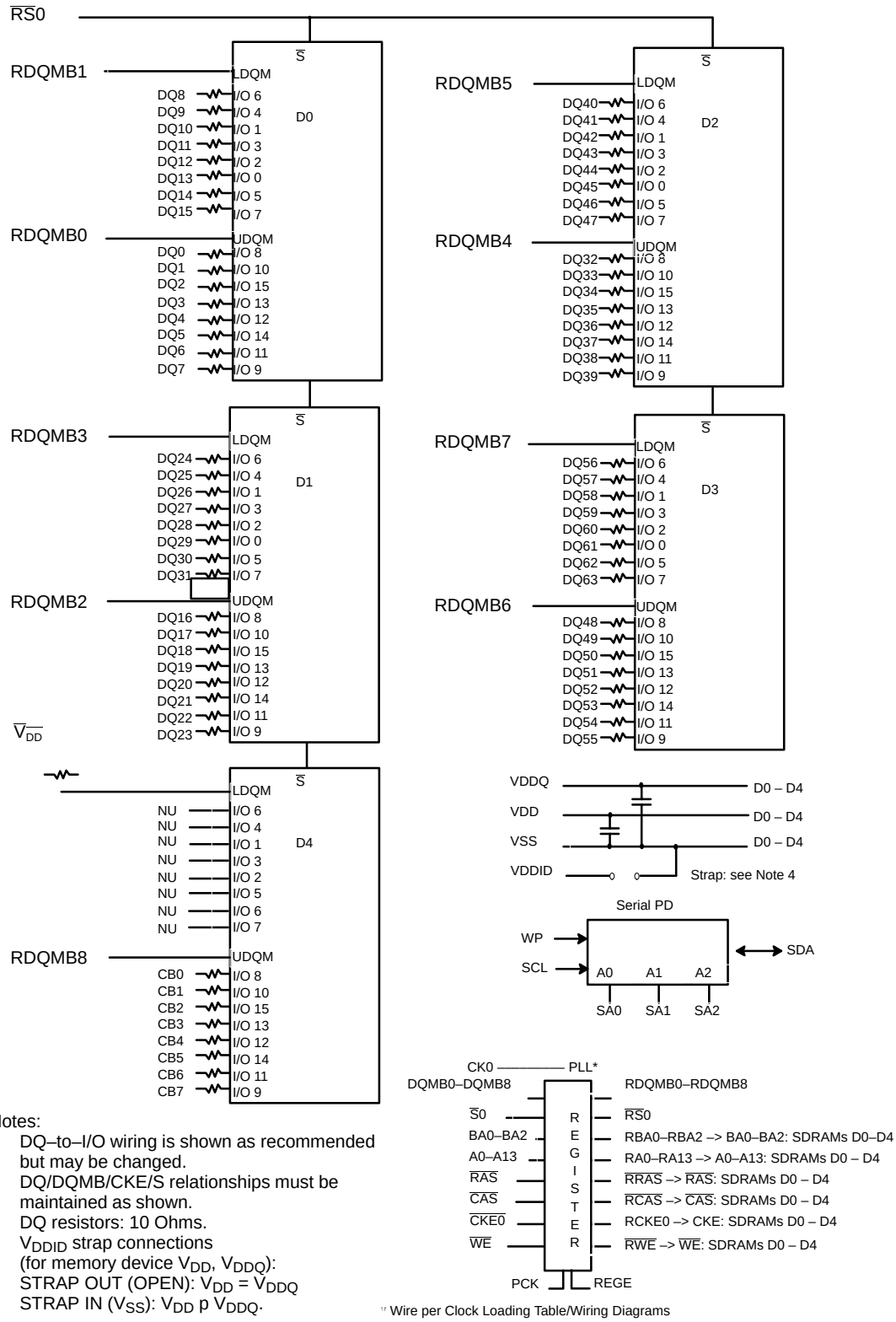
**FIGURE 4.5.12–I**
**184 PIN X72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM**
**(1 BANK, X4 SDR SDRAMS)**




Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections
(for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

* Wire per Clock Loading Table/Wiring Diagrams

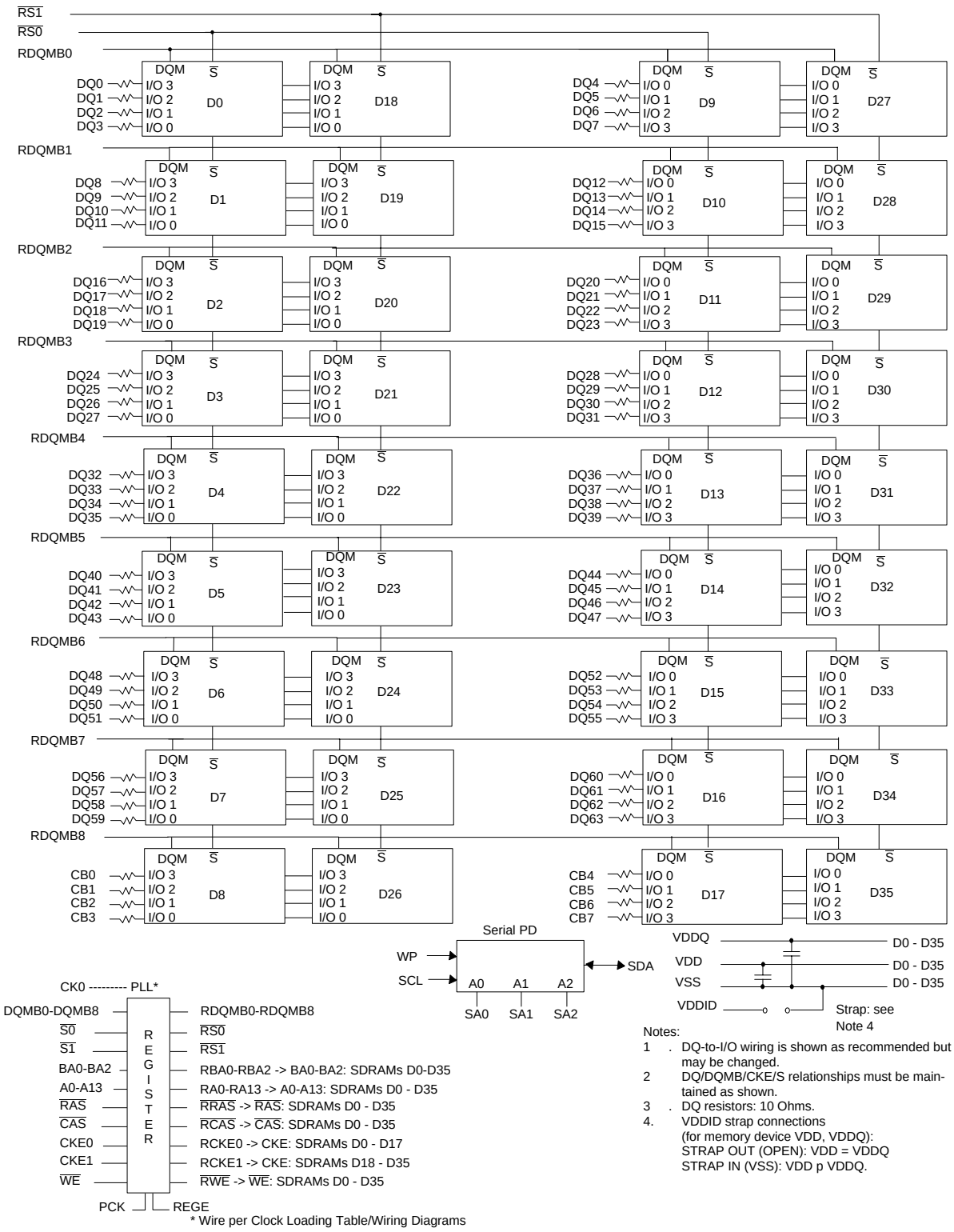
**FIGURE 4.5.12–J**
**184 PIN X 72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM**
**(1 BANK, X 8 SDR SDRAMS)**



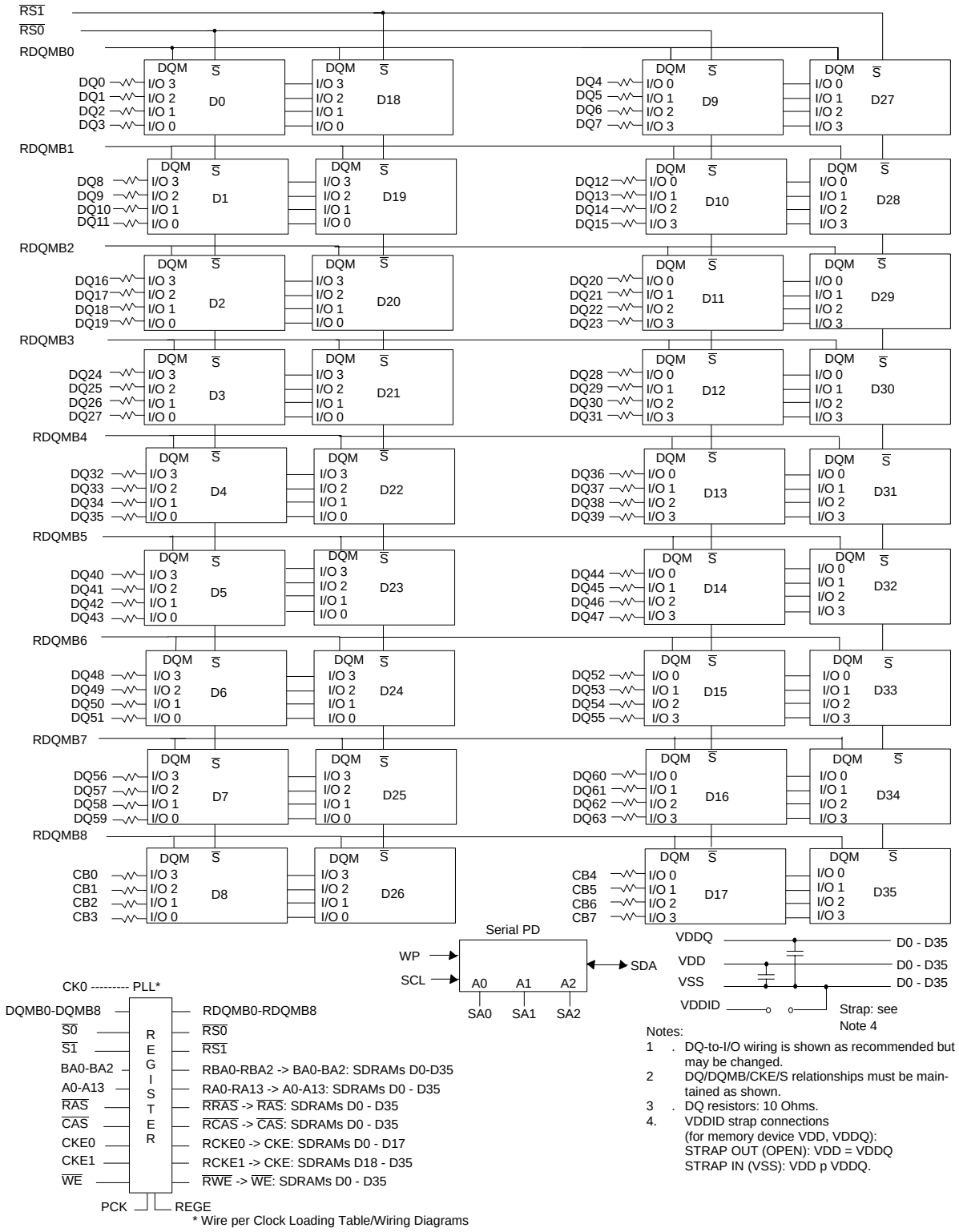

Notes:
1 DQ–to–I/O wiring is shown as recommended but may be changed.
2 DQ/DQMB/CKE/S relationships must be maintained as shown.
3 DQ resistors: 10 Ohms.
4 $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN ($V_{SS}$): $V_{DD}$ p $V_{DDQ}$.

[1] Wire per Clock Loading Table/Wiring Diagrams

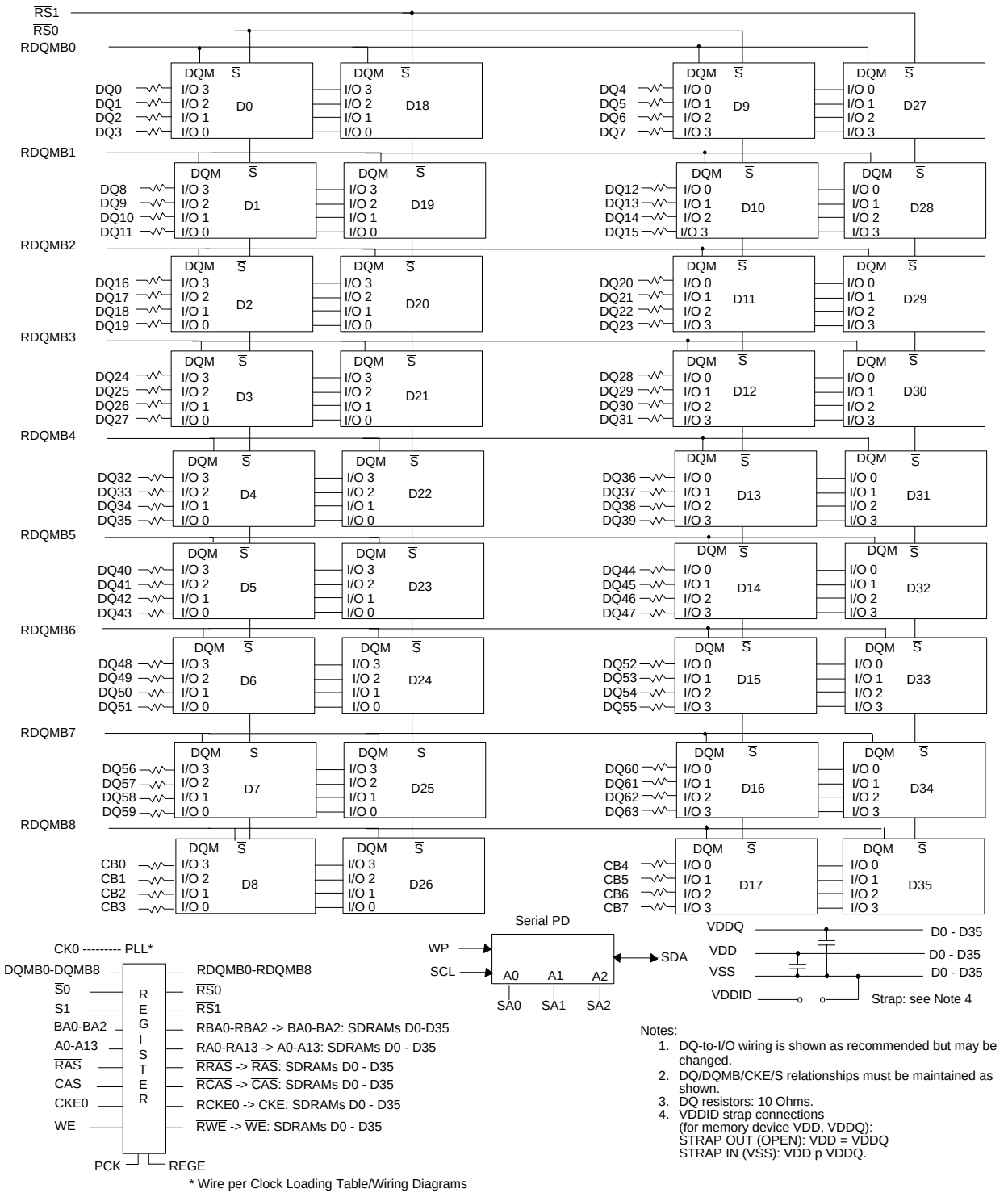
**FIGURE 4.5.12–K**
**184 PIN X 72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM**
**(1 BANK, X 16 SDR SDRAMS)**




# FIGURE 4.5.12–L
# 184 PIN X72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (2 BANKS, X4 SDR SDRAMS WITH DOUBLE CKE)



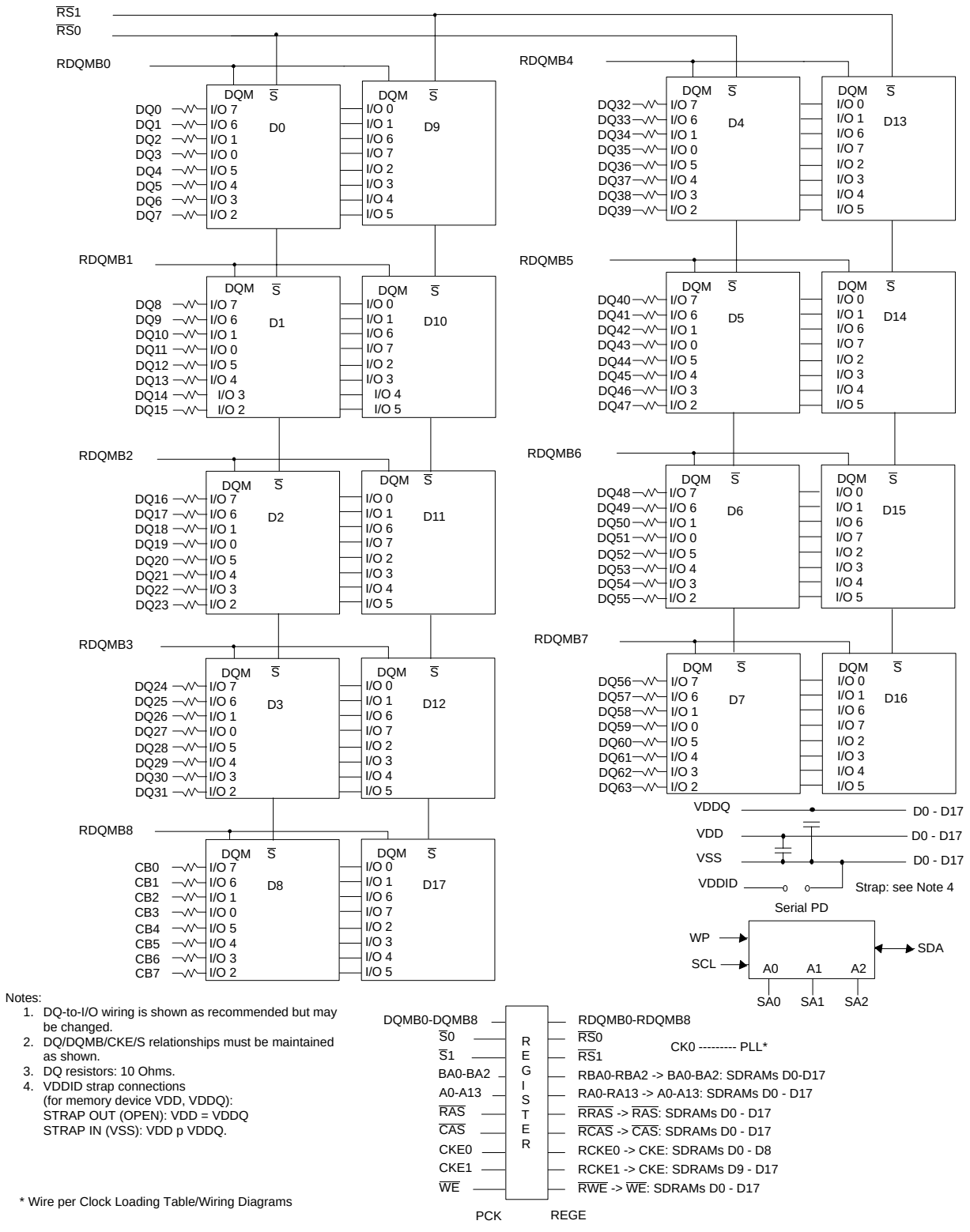

# FIGURE 4.5.12–M
# 184 PIN X72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM
# (2 BANKS, X4 SDR SDRAMS WITH DOUBLE CKE)




* Wire per Clock Loading Table/Wiring Diagrams

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQMB/CKE/S relationships must be maintained as shown.
3. DQ resistors: 10 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ): STRAP OUT (OPEN): VDD = VDDQ STRAP IN (VSS): VDD p VDDQ.

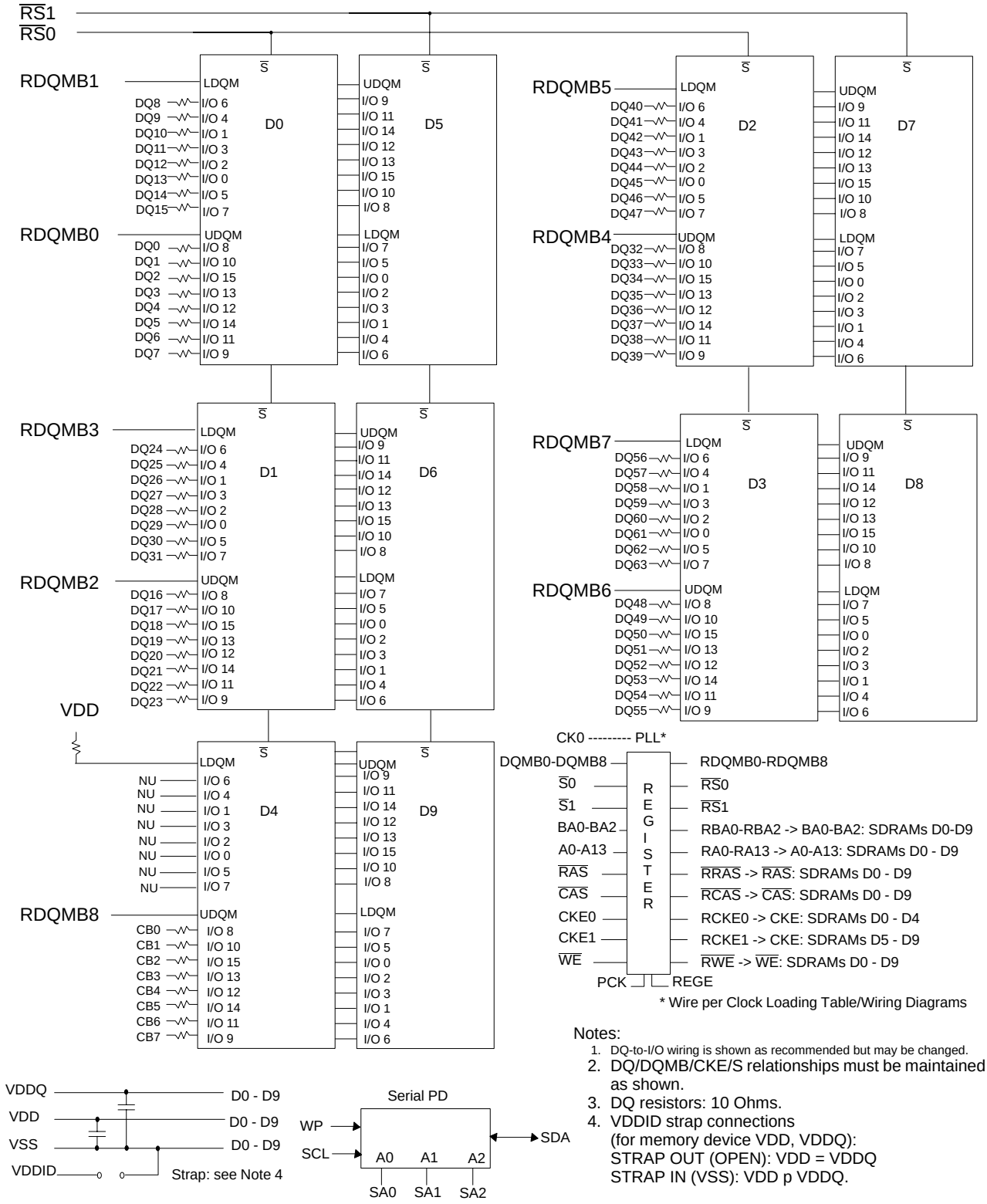
## FIGURE 4.5.12–N
## 184 PIN X72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (2 BANKS, X4 SDR SDRAMS WITH SINGLE CKE)




Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQMB/CKE/S relationships must be maintained as shown.
3. DQ resistors: 10 Ohms.
4. VDDID strap connections
   (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD p VDDQ.

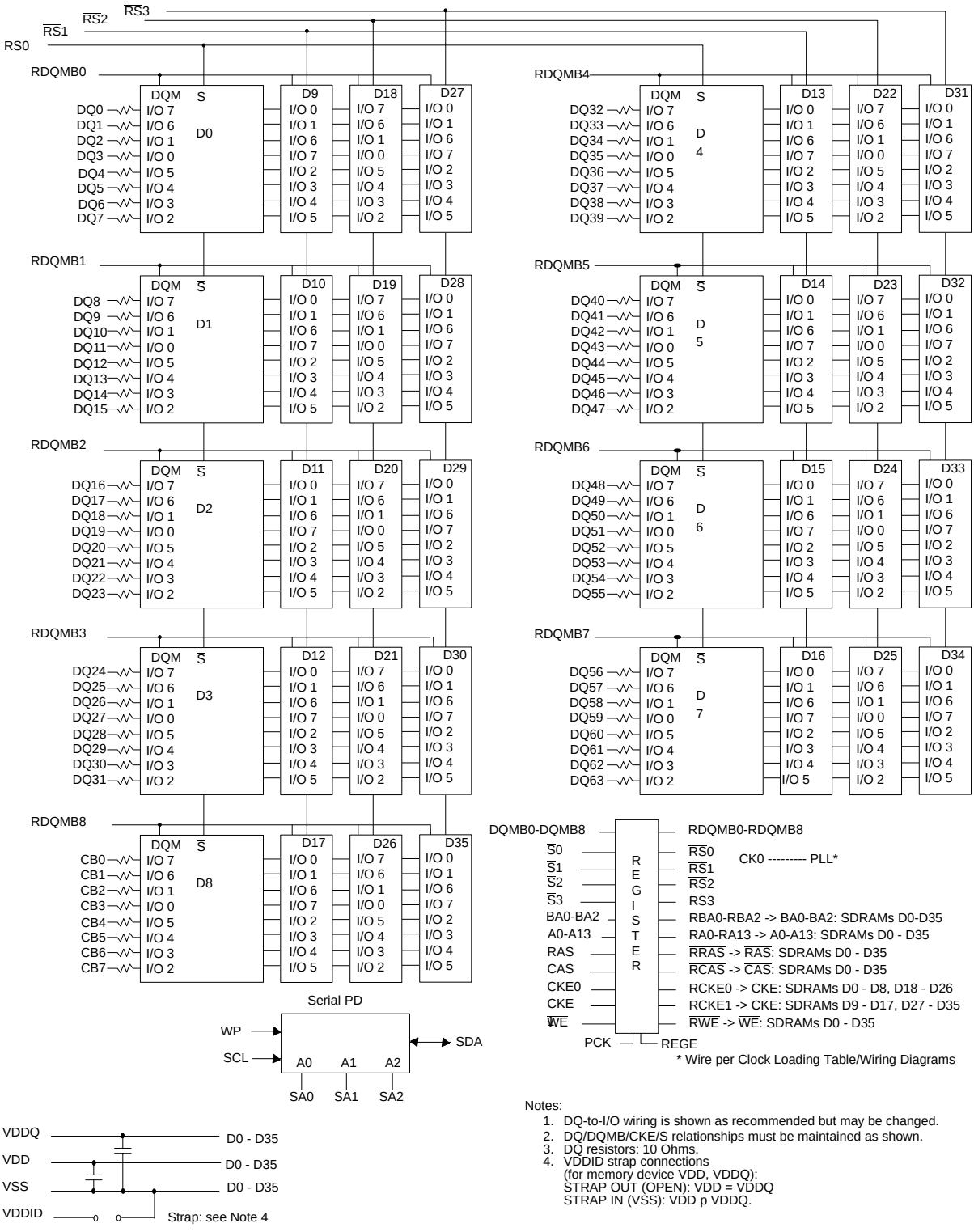
* Wire per Clock Loading Table/Wiring Diagrams

# FIGURE 4.5.12–O
# 184 PIN X72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM
# (2 BANK, X8 SDR SDRAMS)




Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQMB/CKE/S relationships must be maintained as shown.
3. DQ resistors: 10 Ohms.
4. VDDID strap connections
   (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD p VDDQ.

## FIGURE 4.5.12–P
## 184 PIN X72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM
## (2 BANK, X16 SDR SDRAMS)



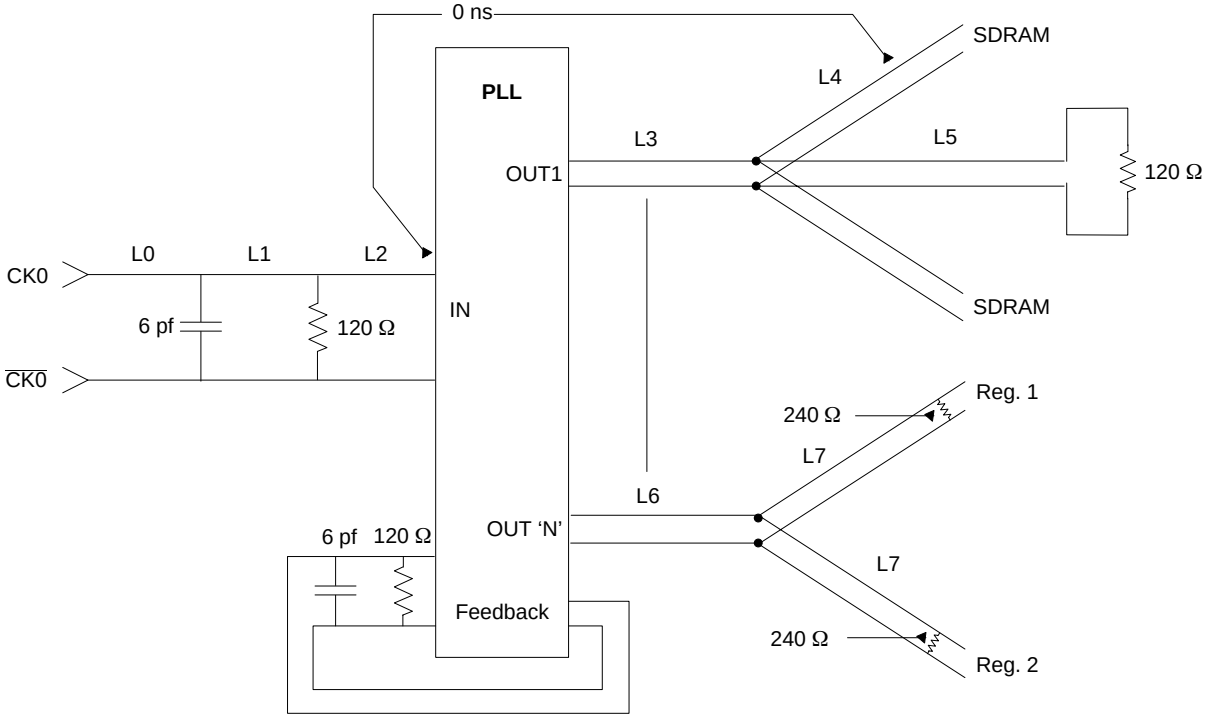

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQMB/CKE/S relationships must be maintained as shown.
3. DQ resistors: 10 Ohms.
4. VDDID strap connections
   (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD p VDDQ.

# FIGURE 4.5.12–Q
# 184 PIN X72 ECC SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM
# (4 BANK, X8 SDR SDRAMS)

## 4.5.12.2 – 184 PIN DIMM Clock Topology

DDR Registered DIMM Clock Network
DDR Unbuffered DIMM Clock Topology

## 184 Pin DDR Registered DIMM Clock Topology



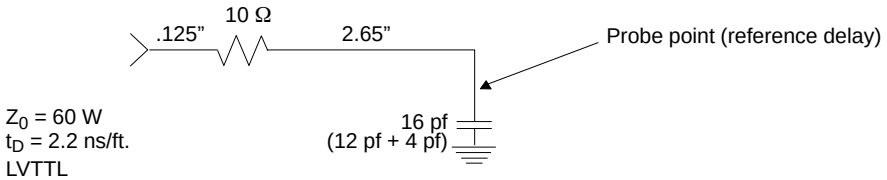

## Recommended Wire Lengths

L0 = Select length to match 'reference net' delay.
L1 = .07" (This length should be as short as possible.)
L2 = .15" (This length should be as short as possible.)
L3 = 2.6"
L4 = .3"
L5 = .6"
L6 = .5" (This length should be selected to ensure identical clock delay to the SDRAM clock.)
L7 = 1.5"

Notes: Notes:

1 Missing DRAM clock input capacitance "C": Cap. = 1/2 of SDRAM clock capacitance and is connected across CK and $\overline{CK}$.
2 Characteristic impedance: $Z_0$ = 60 Ω (approx.) line to common and 60 Ω (approx.) line to line.
3 CK0/$\overline{CK0}$ will be the only clock input pair used on Registered DIMMs.
4 The clock delay from tabs CK0/$\overline{CK0}$ will be identical to the delay on the 168 Pin PC100 and PC133 Registered DIMMs, thereby permitting system designs that support multiple module families.
5 The clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns (nominal). This can be accomplished by setting the PLL feedback wire length and padding capacitance equal to that of the SDRAM clock net. This delay value is identical to the 168 Pin PC100 and PC133 Registered DIMMs.
6 Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.

## Clock Reference Net

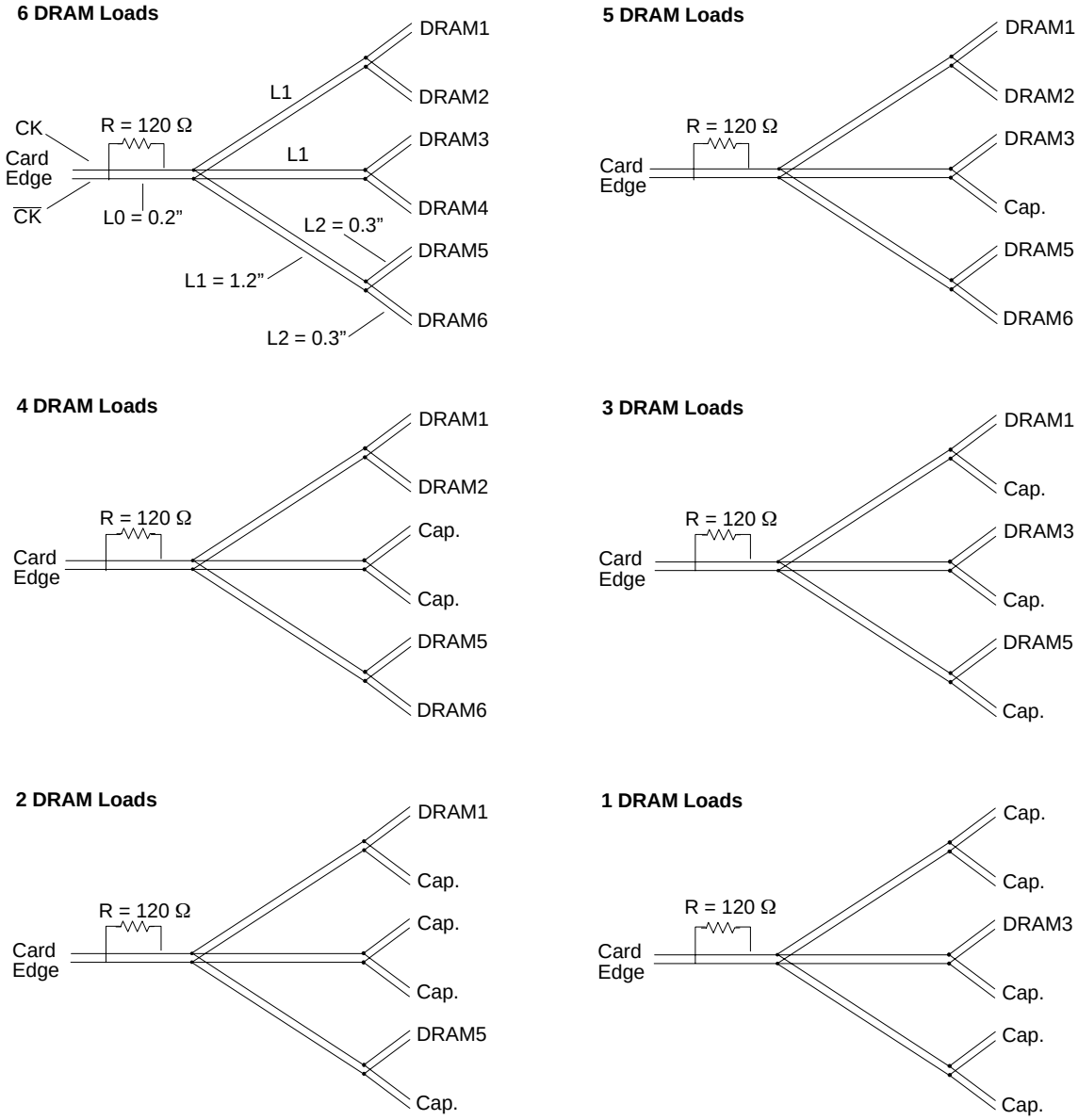



**Note**: Simulation and hardware analysis will compare the LVTTL 1.5V crosspoint in the rising edge of the clock reference net to the differential crosspoint on the rising edge of the DDR clock net (at the load).

# FIGURE 4.5.12–R
# 184 PIN DDR REGISTERED DIMM CLOCK NETWORK

# 184 Pin DDR Unbuffered DIMM Clock Topology

## 184 Pin DDR SDRAM DIMM Clock Net Wiring




Notes: Notes:

7. Wire lengths are for reference and are intended as initial design values. Wire lengths for L0 and L1 must be adjusted to match delay of reference net.
8. Missing DRAM clock input capacitance “C”: Cap. = 1/2 of SDRAM clock capacitance and is connected across CK and $\overline{CK}$.
9. Characteristic impedance: $Z_0$ = 60W (approx.) line to common and 60W (approx.) line to line.

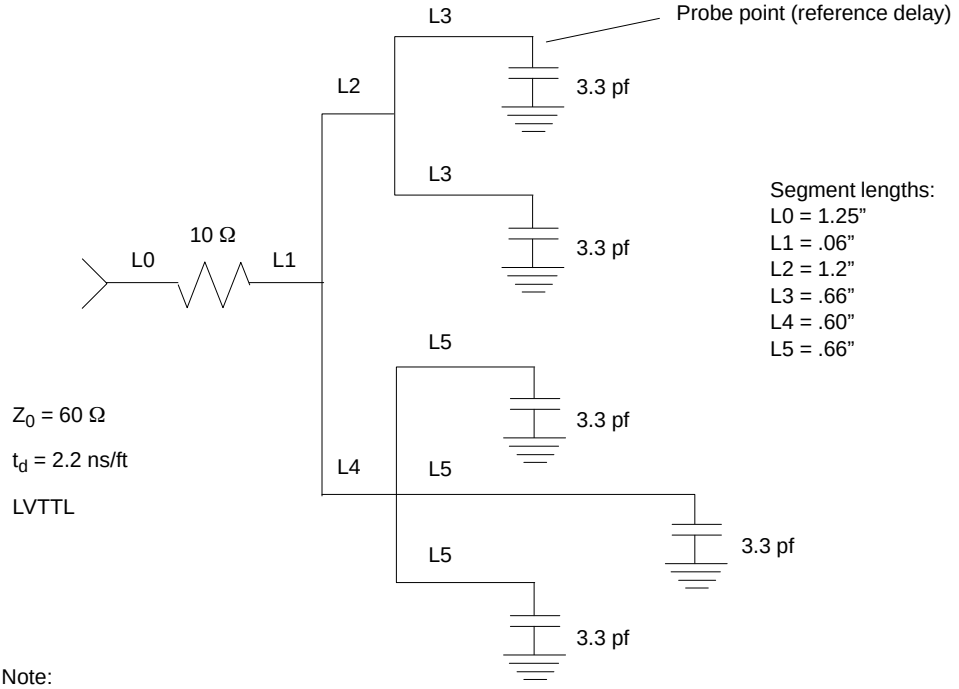
## FIGURE 4.5.12–Sa
## 184 PIN DDR UNBUFFERED DIMM CLOCK NETWORK

## Clocking Assumptions

- Each clock input will wire to six DRAMs or the electrical equivalent.
- Nets with fewer than six DRAMs should use discrete capacitors in lieu of SDRAMs. The capacitor should match 1/2 of the nominal SDRAM clock capacitance and connect across CK and $\overline{CK}$.
- The clock delay from the tab pin to the input of any SDRAM should match the delay on the 168 Pin PC100 Unbuffered DIMM.

A reference net is shown below for simulation and hardware validation purposes.

## Clock Reference Net (168 Pin PC100 Unbuffered DIMM)




Note:
Simulation and hardware analysis will compare the LVTTL 1.5 V crosspoint on the rising edge of the reference net to the differential crosspoint on the rising edge of the DDR clock net (at the load).

**FIGURE 4.5.12–Sb**
**184 PIN DDR UNBUFFERED DIMM CLOCK NETWORK**

### 4.5.12.3 – 184 PIN DDR Registered DIMM Pinout

This pinout is a modification of the pinout of the Unbuffered DDR DIMM pinout given in Section 4.5.10. Pin 10 is changed from ”NC” to ”NU, $\overline{\text{RESET}}$”

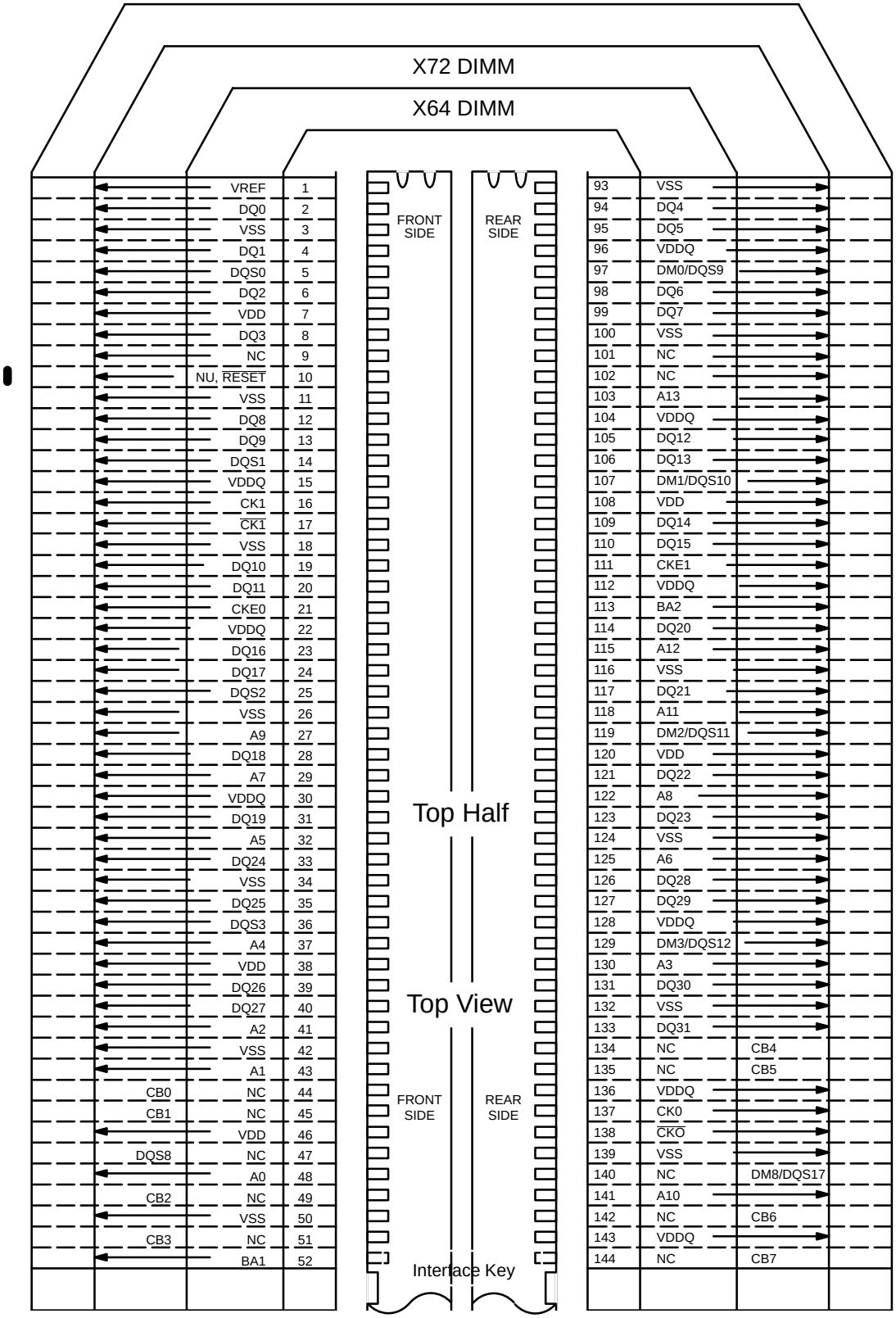



**Figure 4.5.12–Ta**
**184 PIN, 64, OR 72 BIT REGISTERED DDR SDRAM DIMM PINOUT, TOP HALF**

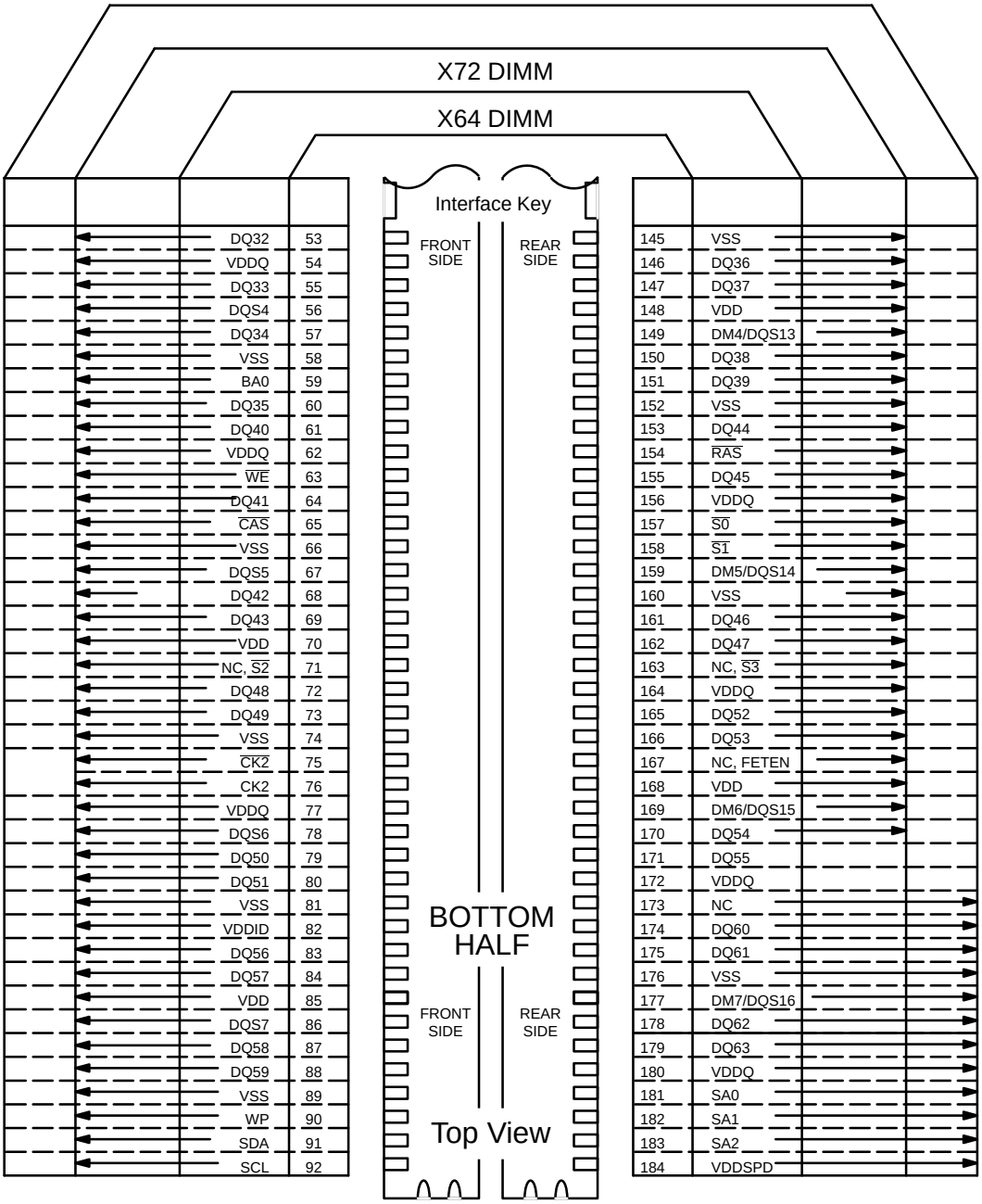



**Figure 4.5.12–Tb**
**184 PIN, 64, OR 72 BIT REGISTERED DDR SDRAM DIMM PINOUT, BOTTOM HALF**